Mentor Graphics IC Studio 2008.1

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Modification for Mentor Graphics IC Studio 2008.1

Setup & Preparation

Add the following lines in your .profile:
setup mentor-2008.1
alias swd="export MGC_WD=\'pwd\'"

Circuit Entry

Specifying Location Map
On the next window that sol/ic_flow

- Click the Open Location Map Editor button. The Location Map Editor.
    - To Add the *design kit's standard cell libraries* to the location map

Click Edit Menu > Add Standard MGC Libraries pull down menu item.
Following libraries will be automatically added.
/opt/mentor-2008.1/sol/ic_flow/2008.1_sun4os5/icflow_home/mgc_icstd_lib/mgc_ic_commlib
/opt/mentor-2008.1/sol/ic_flow/2008.1_sun4os5/icflow_home/mgc_icstd_lib/mgc_ic_comm_qs
/opt/mentor-2008.1/sol/ic_flow/2008.1_sun4os5/icflow_home/mgc_icstd_lib/mgc_ic_comm_rf
/opt/mentor-2008.1/sol/ic_flow/2008.1_sun4os5/icflow_home/mgc_icstd_lib/device_lib
/opt/mentor-2008.1/sol/ic_flow/2008.1_sun4os5/icflow_home/mgc_icstd_lib/generic_lib
/opt/mentor-2008.1/sol/ic_flow/2008.1_sun4os5/icflow_home/mgc_icstd_lib/sources_lib
/opt/mentor-2008.1/sol/ic_flow/2008.1_sun4os5/icflow_home/mgc_icstd_lib/mgc_ic_verilog
/opt/mentor-2008.1/sol/ic_flow/2008.1_sun4os5/icflow_home/mgc_icstd_lib/mgc_ic_macrolib

- Add the *MGC design kit* to the location map

Click Edit Menu > Add MGC Design Kit.
Specify MGC Design Kit path as **/opt/mentor-2008.1/adk3_1**

Specifying Process files and other settings

- Click Open Settings Editor button. The Project tab of the Preferences dialog box appears.
- Load the process file (tsmc0XX). Process files are present in

/opt/mentor-2008.1/adk3_1/technology/ic/process

- Load the following rules file to the project (tsmc0XX.rules)

Rules files are present in **/opt/mentor-2008.1/adk3_1/technology/ic/process**
o DRC rules file: tsmc0XX.rules
o LVS rules file: tsmc0XX.calibre.rules
o SDL rules file: tsmc0XX.accusim.rules
o PEX rules file: tsmc0XX.calibre.rules
NOTE: Select value for XX from 18, 25, and 35 depending on design requirement

- Click OK on the Preferences dialog box.

Modifying Property

NMOS: ASIM_MODEL: N (Required For Simulation)

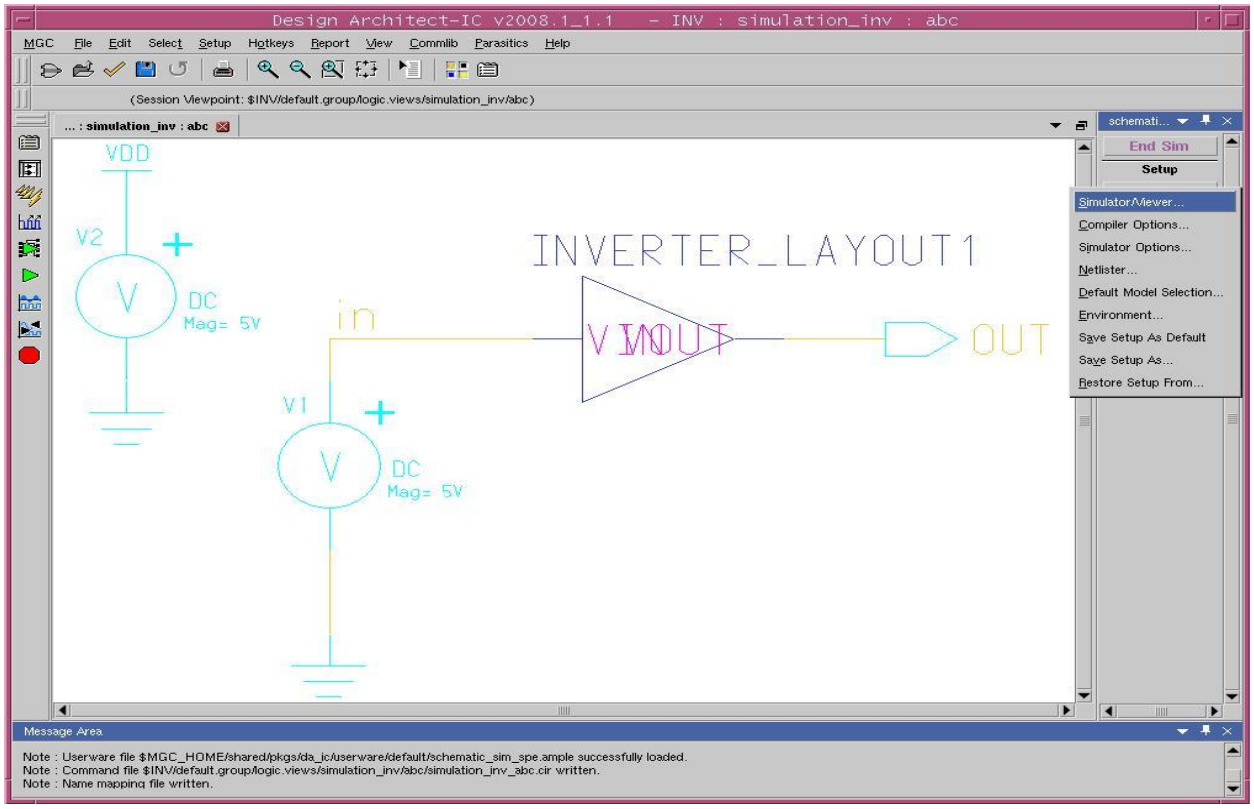
PMOS: ASIM_MODEL: P (Required For Simulation)

Creating a Symbol
Make sure that the schematic is checked & saved before making the symbol.
To generate a Symbol Automatically select **Miscellaneous -> Generate Symbol**

Simulation

Setting up the simulation parameters
In the simulation mode (schematic_sim palette),

- Click the right mouse button Session



- Setup Simulator/Viewer
- Select Eldo and Click OK.

In the simulation mode (schematic_sim palette),

- Click the right mouse button Lib/Temp/Inc

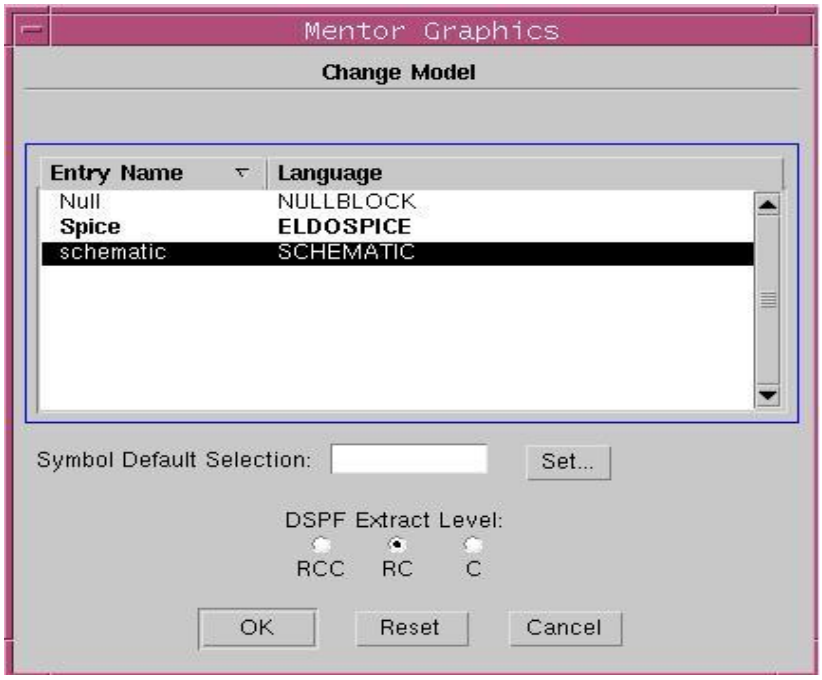
Library:

- Type **/opt/mentor-2008.1/adk3_1/**technology/ic/models/tsmc035.mod in

Library path box and click OK.
This includes the TSMC0.35 micron BSIM model for the simulations.

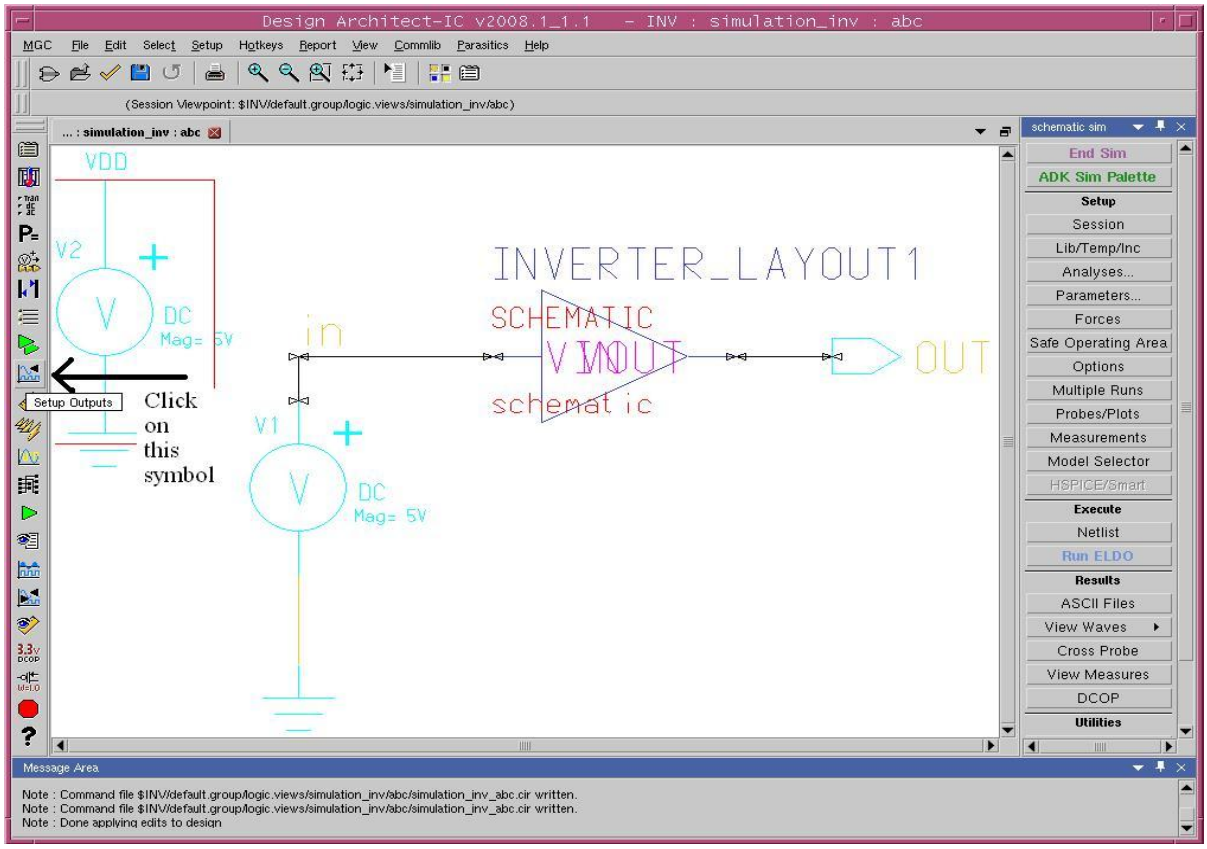
Change Model:

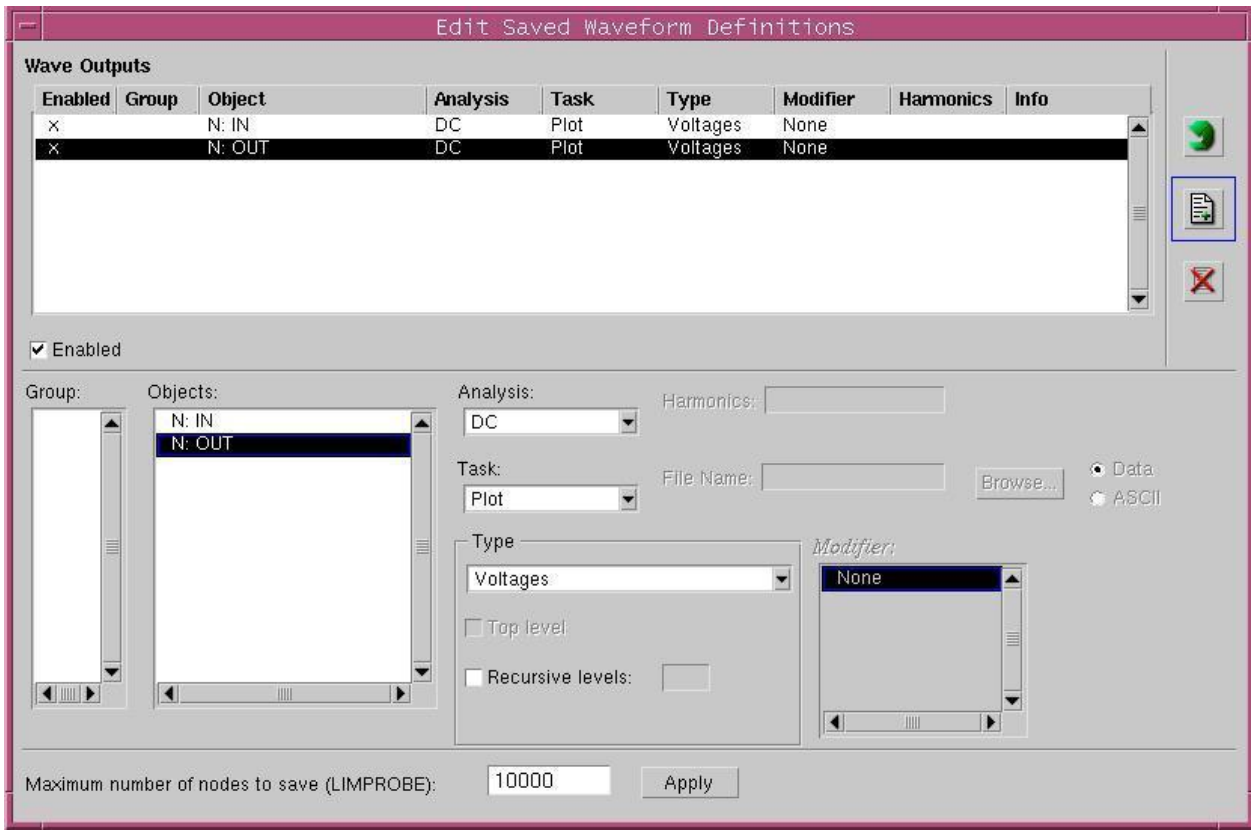
- Right click on the Inverter Symbol:
- Select Schematic.



Probe Output:

- Select the wires connected to INPUT and OUTPUT pins on the sheet.
- From the Menu Bar opens the Set dialog box as shown in the next figure
- Select Object:
    - Analysis: DC
    - Task: Plot
    - Type: Voltage


Design Architect-IC v2008.1_1.1 - INV : simulation_inv : abc
MGC File Edit Select Setup Hotkeys Report View Commlib Parasitics Help
(Session Viewpoint: $INV/default.group/logic.views/simulation_inv/abc)
... : simulation_inv : abc
VDD
V2
DC
Mag= 5V
Setup Outputs
Click on this symbol
V1
DC
Mag= 5V
in
INVERTER_LAYOUT1
SCHEMATIC
schematic
OUT
schematic sim
End Sim
ADK Sim Palette
Setup
Session
Lib/Temp/Inc
Analyses...
Parameters...
Forces
Safe Operating Area
Options
Multiple Runs
Probes/Plots
Measurements
Model Selector
HSPICE/Smart
Execute
Netlist
Run ELDO
Results
ASCII Files
View Waves
Cross Probe
View Measures
DCOP
Utilities
Message Area
Note : Command file $INV/default.group/logic.views/simulation_inv/abc/simulation_inv_abc.cir written.
Note : Command file $INV/default.group/logic.views/simulation_inv/abc/simulation_inv_abc.cir written.
Note : Done applying edits to design


Edit Saved Waveform Definitions
Wave Outputs
Enabled
Group
Object
Analysis
Task
Type
Modifier
Harmonics
Info
N: IN DC Plot Voltages None
N: OUT DC Plot Voltages None
Enabled
Group:
Objects:
N: IN
N: OUT
Analysis:
DC
Harmonics:
Task:
Plot
File Name:
Browse...
Data
ASCII
Type
Voltages
Top level
Recursive levels:
Modifier:
None
Maximum number of nodes to save (LIMPROBE):
10000
Apply

Run DRC

From the menu, select **Calibre > Run DRC**
In the window that pops up, enter the **Path to Calibre as:**
/opt/mentor-2008.1/adk3_1/technology/ic/process/tsmc035.rules

Run LVS

From the menu, select **Calibre > Run LVS**
In the window that pops up, enter the **Path to Calibre as:**
/opt/mentor-2008.1/adk3_1/technology/ic/process/tsmc035.calibre.rules